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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/430,366
Filing Date	Oct 28, 1999
First Named Inventor	Ramsbey, Mark T.
Art Unit	2813
Examiner Name	Chen, Jack S.J.
Attorney Docket Number	0180164
Total Number of Pages in This Submission	

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
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- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] CD, Number of CD(s) ________
- [ ] After Allowance communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
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2. Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Michael, Farjami, Esq., Reg. No. 38,135 Farjami & Farjami LLP
Signature	[signature]
Date	May 14, 2004

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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/430,366
Filing Date	10/28/1999
First Named Inventor	Ramsbey, et al.
Examiner Name	Chen, Jack S.J.
Art Unit	2813
Attorney Docket No.	0180164

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☒ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 50-0731

Deposit Account Name: Farjami & Farjami LLP

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20**=		X		=	
Independent Claims		- 3**=		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

*** or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) ______________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)330.00

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Michael Farjami, Esq.	*Registration No. (Attorney/Agent)*	38135	*Telephone*	(949) 282-1000
Signature	[signature]			*Date*	5/14/04

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Attorney Docket No.: 0180164

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ramsbey, et al.

Serial No.: 09/430,366

Filed: October 28, 1999

For: **Method Of Making A Memory Cell With Polished Insulator Layer**

Art Unit: 2813

Examiner: Chen, Jack S. J.

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1, 4, 5, 7, 9-11, 14, 15, and 23. The Final Rejection issued on November 14, 2003. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on March 15, 2004.

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1, 4-5, 7, 9-11, 14-15, and 23 are pending, and claims 2-3, 6, 8, 12-13, and 16-22 were canceled in previous amendments. Claims 1, 4-5, 7, 9-11, 14-15, and 23 have been finally rejected in a Final Rejection dated November 14, 2003. This Appeal is directed to the rejection of claims 1, 4-5, 7, 9-11, 14-15, and 23. Claims 1, 4-5, 7, 9-11, 14-15, and 23 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments were submitted on February 3, 2004 in response to the Final Rejection dated November 14, 2003.

SUMMARY OF INVENTION

A. Brief Description

The present invention relates to a method for fabricating a flash memory cell, wherein the planarity of a dielectric layer and a control gate layer deposited on the

floating gate of the flash memory cell are improved in order to facilitate patterning of the dielectric and control gate layers. As disclosed in the present application, a process for fabricating flash memory cell 10 includes forming tunnel oxide layer 14 on substrate 22, depositing floating gate layer 16 on tunnel oxide layer 14, and etching floating gate layer 16. Page 4, lines 1-12 and Figures 3 and 4 of the present application. As disclosed in the present application, insulator 30 is deposited on substrate 22 such that insulator 30 covers floating gate layer 16 and is in contact with vertical side surfaces 17 of floating gate layer 16. Page 4, lines 19-24 and Figure 5 of the present application.

As further disclosed in the present application, "[i]nsulator 30 is preferably a high quality oxide which will prevent charge from leaking out of vertical side surfaces 17 of floating gate 16." Page 4, lines 25-26 of the present application. For example, a high temperature oxide, such as LPCVD furnace grown oxide, is a high quality oxide. Page 4, lines 26-27 of the present application. Thus, by utilizing a high quality oxide, such as an oxide formed by a LPCVD process, to form insulator 30, the present invention advantageously prevents charge from leaking out of vertical side surfaces 17 of floating gate 16. As further disclosed in the present application, other insulator materials, such as nitride, silicon oxide, or a spin-on-glass (SOG) can also be used for insulator 30 if floating gate 16 undergoes an optional thermal oxidation process to seal vertical side surfaces 17 prior to deposition of insulator 30. Page 4, lines 15-18 and lines 27-30 of the present application.

Next, insulator 30 is polished using chemical-mechanical polishing techniques until thickness T_2 of second region 34 of insulator 30 is substantially equal to thickness T_1 of floating gate 16, which results in a planar layer of floating gate 16 and insulator 30 on tunnel oxide layer 14. Page 4, lines 31-31, page 5, lines 1-4, and Figure 6 of the present application. As further disclosed in the present application, dielectric layer 18, which can be an ONO layer, and control gate layer 20 are deposited on the planar surface over the top surface of floating gate 16 and insulator 30 and etched to provide a stacked gate structure. Page 5, lines 5-19 and Figure 1 of the present application.

Since floating gate 16 and insulator 30 form a planar layer as discussed above, little variation in thickness occurs along the deposited dielectric and control gate layers. As a result, the process of the present invention advantageously facilitates removal of the dielectric and control gate layers during the etch process. Page 5, lines 24-26 of the present application.

B. Claim 1 and its dependent claims

The method of independent claim 1 claims, among other things, depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating

gate and the insulator layer, and depositing an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

Dependent claims 4 and 5 specify embodiments of the method of independent claim 1. Claim 4 specifies that the insulator layer, such as insulator 30, is polished using chemical mechanical polishing, and claim 5 specifies depositing a control gate layer, such as control gate layer 20, on the ONO layer and etching the control gate layer and the ONO layer to form a stacked gate structure of the flash memory cell, as shown in Figure 1 of the present application.

C. Claim 7 and its dependent claims

The method of independent claim 7 claims, among other things, depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process, polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer, and depositing an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

Dependent claims 9-11 and 14-15 specify various embodiments of the method of independent claim 7. Claim 9 specifies that a first thickness, such as T_1, of the floating gate layer is between 500 Angstroms and 2000 Angstroms, and a second thickness, such

as T_2, of the insulator layer is between approximately 1000 Angstroms and 5000 Angstroms. Claim 10 specifies that the insulator layer, such as insulator 30, is polished using chemical mechanical polishing, and claim 11 specifies depositing a control gate layer, such as control gate layer 20, on the ONO layer and etching the control gate layer and the ONO layer to form a stacked gate structure of the flash memory cell, as shown in Figure 1 of the present application. Claims 14 and 15 specify that the floating gate layer comprises doped polysilicon and doped amorphous silicon, respectively.

D. Claim 23

The method of independent claim 23 claims, among other things, depositing an insulator layer comprising a high quality oxide directly on a tunnel oxide layer and a floating gate, where the insulator layer is formed on and in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and where the high quality oxide is formed by a LPCVD process, and polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer.

ISSUES

(1) Whether the Examiner's rejection that claims 1, 4-5, 7, 9-11, 14-15, and 23 on Appeal are unpatentable under 35 U.S.C. §103 over U.S. Patent No. 5,808,339 to Yamagishi et al. ("Yamagishi") taken with "ULSI Technology," 1996, p. 211, by

Sze et al. ("Sze") or U.S. Patent No. 4,613,956 to Paterson et al. ("Paterson") and in view of "Applicant's admitted prior art" is erroneous.

(2) Whether the Examiner's rejection that claims 1, 4-5, 7, 9-11, 14-15, and 23 on Appeal are unpatentable under 35 U.S.C. §103 over U.S. Patent No. 6,033,956 to Shye-Lin Wu ("Wu") or U.S. Patent No. 4,713,142 to Mitchell et al. ("Mitchell") taken with Yamagishi, and in view of Sze or Paterson is erroneous.

(3) Whether the Examiner's rejection that claims 14-15 on Appeal are unpatentable under 35 U.S.C. §103 over Wu or Mitchell taken with Yamagishi and in view of Sze or Paterson as applied to claims 1, 4-5, 7, 9-11, and 23, and further in view of "Applicant's admitted prior art."

GROUPING OF CLAIMS

Claims 1, 4-5, 7, 9-11, 14-15, and 23 stand or fall together, for the reasons set forth in the Argument.

ARGUMENT

(1) The Rejection of Claims 1, 4-5, 7, 9-11, 14-15, and 23

Claims 1, 4-5, 7, 9-11, 14-15, and 23 stand rejected under 35 U.S.C. §103 over Yamagishi taken with Sze or Patterson and in view of "Applicant's admitted prior art." For the reasons discussed below, Appellant respectfully submits that the present

invention, as defined by independent claims 1, 7, and 23, is patentably distinguishable over Yamagishi, Sze, and Patterson, considered singly or in any combination thereof.

In contrast to the present invention as defined by independent claim 1, Yamagishi does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process. Yamagishi specifically discloses forming first gate insulating layer 51 on element formation region 12 of semiconductor substrate 11, forming electrode pattern 53 over first gate insulating layer 51, and forming second insulating layer 54 over electrode pattern 53 and element isolation region 13. See, for example, column 12, lines 11-30 and Figures 9A-9E of Yamagishi. In Yamagishi, first gate insulating layer 51 is formed on element formation region 12 by a heat oxidation method and second insulating layer 54 is formed by a CVD method. See, for example, Yamagishi, column 12, lines 11-14 and lines 27-28.

However, in Yamagishi, since electrode pattern 53 covers first gate insulating layer 51 (as shown in Figure 9D of Yamagishi), second insulating layer 54 is not depositing directly on first gate insulating layer 51. Furthermore, Yamagishi fails to teach, disclose, or suggest depositing an insulator layer directly on exposed portions of a tunnel oxide layer and a floating gate, as specified in independent claim 1. Additionally, in Yamagishi, second insulating layer 54 is formed by a CVD method. However, Yamagishi fails to

teach, disclose, or suggest an insulating layer comprising a high temperature oxide and being formed by a LPCVD process directly on exposed portions of a tunnel oxide layer and the floating gate, as specified by independent claim 1.

On page 3 of the Final Rejection dated November 14, 2003, the Examiner states that Figure 9E, column 12, lines 27-31 of Yamagishi "inherently shows the CVD oxide is the high temperature/quality oxide" and "it should be noted that LPCVD is a type of CVD process." However, independent claim 1 specifically requires an insulator layer comprising a high temperature oxide, where the insulator layer is formed by a LPCVD process. Appellant respectfully submits that a LPCVD process produces a high temperature oxide, while, as is known in the art, a CVD process could produce a low temperature oxide. Thus, a CVD process specification or limitation is not the same as a LPCVD process specification or limitation.

The Examiner also states that "applicant stated in the specification, other dielectric may [*sic*] used, i.e. see page 3, lines 26-30," and further states "the disclosure fails to mention the criticality of the LPCVD process." Page 4 of the Final Rejection dated November 14, 2003. However, as disclosed in the present application, other insulator materials can be used **if** the floating gate undergoes an optional thermal oxidation to seal side surfaces 17 of floating gate 16 prior to deposition of insulator 30. Page 4, lines 15-19 and lines 27-30 of the present application (emphasis added). Also, as disclosed in the present application, insulator 30 is preferably a high quality oxide, such as LPCVD furnace grown oxide, to prevent charge from leaking out of vertical side surfaces 17 of

floating gate 16. Page 4, lines 25-27 of the present application. Thus, the LPCVD oxide is utilized in the present invention to sufficiently seal the vertical side surfaces 17 of floating gate 16 to prevent charge leakage. Thus, Appellant respectfully submits that the present application discloses the criticality of a high quality oxide, such as LPCVD oxide, for preventing charge from leaking out of the vertical side surfaces of the floating gate.

Moreover, Yamagishi does provide any motivation for forming LPCVD oxide on the vertical sidewall surfaces of a floating gate, such as preventing charge leaking from the floating gate. Thus, Yamagishi has failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which are also not disclosed or suggested in Sze and Paterson.

Sze is cited by the Examiner to teach forming a dielectric by using a LPCVD process to provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput. Page 4 of the Final Rejection dated November 14, 2003. However, Sze also teaches that the LPCVD process has disadvantages, such as high temperature and low deposition rate. See, for example, page 211, Table 1 of Sze. Furthermore, Sze fails to teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the

floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process. Thus, Sze fails to remedy the basic deficiencies of Yamagishi discussed above. In other words, Yamagishi has failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which is also not disclosed or suggested in Sze.

Paterson is also cited by the Examiner to teach "a method of forming a semiconductor device, which includes depositing a high/temperature/quality oxide on the floating gate by LPCVD in order to provide high uniformity and a highly doped floating gate (col. 3, lines 65-col. 4, lines 6 and col.4 line 67-col. 5, line 47)." Page 4 of the Final Rejection dated November 14, 2003. In Patterson, a composite oxide/nitride/oxide dielectric is deposited on a floating gate by a LPCVD process in order to provide high uniformity and a highly doped first polysilicon gate. See, for example, Paterson, column 3, lines 54-68, and column 4, lines 1-6. However, Paterson does not teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process. Furthermore, Paterson does not teach, disclose, or suggest utilizing an insulator formed by a LPCVD process and

covering the sides of a floating gate such that the LPCVD-formed insulator prevents charge from leaking out of the sides of the floating gate.

Thus, Paterson fails to overcome the deficiencies of Yamagishi discussed above. In other words, Yamagishi has failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which is also not disclosed or suggested in Paterson.

The Examiner has stated that it would have been obvious to use LPCVD oxide as taught by Sze or Paterson in the method of Yamagishi in order to provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput. Page 4 of the Final Rejection dated November 14, 2003. The Appellant disagrees and submits that the Examiner has failed to provide any motivation that is disclosed or suggested in Yamagishi to modify the method in Yamagishi to specifically use LPCVD oxide as taught by Sze or Paterson on the vertical side surfaces of the floating gate. Furthermore, any motivation to modify the method in Yamagishi to use LPCVD oxide as taught by Sze or Paterson would have to be sufficiently strong in order to overcome the disadvantages of using a LPCVD process as also taught in Sze, such as high temperature and low deposition rate.

Thus, considered together, the collective teachings of Yamagishi, Sze, and Paterson do not and cannot result in the present claimed invention. The purported combination of Yamagishi, Sze, and Paterson suggested by the Examiner is not based on anything that can be gleaned from the teachings of these references considered together. Rather, the teachings suggested by the Examiner are based on a classic hindsight reconstruction given the benefit of Appellant's disclosure, which is impermissible.

For the foregoing reasons, Appellant respectfully submits that the present invention, as disclosed by independent claim 1, is not suggested, disclosed, or taught by Yamagishi, Sze, and Paterson, either singly or in combination thereof. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over Yamagishi, Sze, and Paterson. Thus, claims 4-5 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The method of independent claim 7 teaches, among other things, depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process. Independent claim 7 specifies limitations similar to those recited in independent claim 1. Thus, for similar reasons as discussed above, Appellant respectfully submits that the present invention, as defined by independent claim 7, is not suggested, disclosed, or

taught by Yamagishi, Sze, and Paterson. As such, the present invention, as defined by independent claim 7, is patentably distinguishable over Yamagishi, Sze, and Paterson. Thus claims 9-11 and 14-15 depending from independent claim 7 are, *a fortiori*, also patentably distinguishable over Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The method of independent claim 23 teaches, among other things, depositing an insulator layer comprising a high quality oxide directly on a tunnel oxide layer and a floating gate, where the insulator layer is formed on and in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and where the high quality oxide is formed by a LPCVD process. Independent claim 23 specifies limitations similar to those recited in independent claim 1. Thus, for similar reasons as discussed above, Appellant respectfully submits that the present invention, as defined by independent claim 23, is not suggested, disclosed, or taught by Yamagishi, Sze, and Paterson. As such, the present invention, as defined by independent claim 23, is patentably distinguishable over Yamagishi, Sze, and Paterson.

(2) The Rejection of Claims 1, 4-5, 7, 9-11, and 23

Claims 1, 4-5, 7, 9-11, and 23 stand rejected under 35 U.S.C. §103 over Wu or Mitchell taken with Yamagishi and in view of Sze or Paterson. For the reasons discussed below, Appellant respectfully submits that the present invention, as defined by

independent claims 1, 7, and 23, is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Patterson, considered singly or in any combination thereof.

In contrast to the present invention as defined by independent claim 1, Wu does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, and polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer. Wu specifically discloses depositing CVD TEOS oxide 210 over polysilicon layer 204 and polysilicon slots 205, spinning planarizing photoresist 212 on the wafer, applying a second resist coat, and utilizing a planarizing plasma etch to etch both CVD TEOS oxide layer 210 and photoresist 212 such that the surface of polysilicon layer 204 is exposed. See, for example, Wu, column 1, lines 46-58.

However, Wu fails to teach, disclose, or suggest an insulator layer comprising a high temperature oxide, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and where the insulator layer is formed by a LPCVD process. Additionally, in Wu, after CVD TEOS oxide layer 210 has been deposited, two photoresist layers 212 are applied and a planarizing plasma etch is utilized to etch both CVD TEOS oxide layer 210 and photoresist layers 212. See,

for example, Wu, column 1, lines 46-57. However, Wu fails to teach, disclose, or suggest polishing the insulator layer immediately after the insulator has been deposited, as specified in independent claim 1.

On page 5 of the Final Rejection dated November 14, 2003, the Examiner states that "CVD oxide inherently shows the oxide is the high temperature oxide and not limited to any particular type CVD methods [i.e. LPCVD, PECVD, etc.], which produces the high temperature/duality oxide." However, independent claim 1 specifically requires an insulator layer comprising a high temperature oxide, where the insulator layer is formed by a LPCVD process. Appellant respectfully submits that a LPCVD process produces a high temperature oxide, while, as is known in the art, a CVD process could produce a low temperature oxide. Thus, a CVD process specification or limitation is not the same as a LPCVD process specification or limitation.

The Examiner also states that "on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results," and further states that "the disclosure fails to mention the criticality of the LPCVD process." Page 5 of the Final Rejection dated November 14, 2003. However, as disclosed in the present application, other insulator materials can be used **if** the floating gate undergoes an optional thermal oxidation to seal side surfaces 17 of floating gate 16 prior to deposition of insulator 30. Page 4, lines 15-19 and lines 27-30 of the present application (emphasis added). Also, as disclosed in the present application, insulator 30 is preferably a high quality oxide, such as LPCVD furnace grown oxide, to prevent charge from leaking out

of vertical side surfaces 17 of floating gate 16. Page 4, lines 25-27 of the present application. Thus, the LPCVD oxide is utilized in the present invention to sufficiently seal the vertical side surfaces 17 of floating gate 16 to prevent charge leakage. Thus, Appellant respectfully submits that the present application discloses the criticality of a high quality oxide, such as LPCVD oxide, for preventing charge from leaking out of the vertical side surfaces of the floating gate.

Moreover, Wu does provide any motivation for forming LPCVD oxide on the vertical sidewall surfaces of a floating gate, such as preventing charge leaking from the floating gate. Thus, Wu has failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which are also not disclosed or suggested in Mitchell, Yamagishi, Sze, and Paterson.

In contrast to the present invention as defined by independent claim 1, Mitchell does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, and polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar

surface that exposes a top surface of the floating gate and the insulator layer. Mitchell specifically discloses subjecting polycrystalline silicon layer 33 and gate oxide layer 32, which are formed in the surface of substrate 1, to thermal oxidation to form silicon dioxide layer 36. See, for example, column 2, lines 64-68, column 3, line 1, and Figure 2b of Mitchell. In Mitchell, silicon dioxide layer 37 is then formed on silicon dioxide layer 36 by using a CVD process. See, for example, column 3, lines 8-11 and Figure 2c of Mitchell.

Thus, in Mitchell, silicon dioxide layer 36 is situated between silicon dioxide layer 37 and polycrystalline silicon layer 33 and gate oxide layer 32. The Examiner states that both silicon dioxide layer 36 and silicon dioxide layer 37 can be considered as an insulating layer. Page 6 of the Office Action dated November 14, 2003. However, silicon dioxide layer 36 is formed by thermal oxidation while silicon dioxide layer 37 is formed by a CVD process. Thus, silicon dioxide layer 36 and silicon dioxide layer 37 are two distinct layers that are formed by completely different processes. Thus, Mitchell fails to teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate. Additionally, Mitchell fails to teach, disclose, or suggest an insulator layer formed in a LPCVD process as specified in independent claim 1. Furthermore, in Mitchell, photoresist layer 38 is formed over silicon dioxide layer 37 before an etch process is performed to expose the surface of polysilicon layer 33. Thus, Mitchell fails to

teach, disclose, or suggest polishing the insulator layer immediately after the insulator layer has been deposited.

On page 6 of the Final Rejection dated November 14, 2003, the Examiner states that "CVD oxide, inherently shows the oxide is the high temperature oxide and not limited to any particular type CVD methods [i.e. LPCVD, PECVD, etc.], which produces the high temperature/quality oxide." However, independent claim 1 specifically requires an insulator layer comprising a high temperature oxide, where the insulator layer is formed by a LPCVD process. Appellant respectfully submits that a LPCVD process produces a high temperature oxide, while, as is known in the art, a CVD process could produce a low temperature oxide. Thus, a CVD process specification or limitation is not the same as a LPCVD process specification or limitation.

The Examiner also states that "on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results," and further states that "the disclosure fails to mention the criticality of the LPCVD process." Page 6 of the Final Rejection dated November 14, 2003. However, as disclosed in the present application, other insulator materials can be used **if** the floating gate undergoes an optional thermal oxidation to seal side surfaces 17 of floating gate 16 prior to deposition of insulator 30. Page 4, lines 15-19 and lines 27-30 of the present application (emphasis added). Also, as disclosed in the present application, insulator 30 is preferably a high quality oxide, such as LPCVD furnace grown oxide, to prevent charge from leaking out of vertical side surfaces 17 of floating gate 16. Page 4, lines 25-27 of the present

application. Thus, the LPCVD oxide is utilized in the present invention to sufficiently seal the vertical side surfaces 17 of floating gate 16 to prevent charge leakage. Thus, Appellant respectfully submits that the present application discloses the criticality of a high quality oxide, such as LPCVD oxide, for preventing charge from leaking out of the vertical side surfaces of the floating gate.

Moreover, Mitchell does provide any motivation for forming LPCVD oxide on the vertical sidewall surfaces of a floating gate, such as preventing charge leaking from the floating gate. Thus, Mitchell has failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which are also not disclosed or suggested in Wu, Yamagishi, Sze, and Paterson.

Yamagishi is cited by the Examiner to teach polishing an insulator layer immediately after the step of depositing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer. Page 8 of the Final Rejection date November 14, 2003. However, as discussed above, Yamagishi has failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge

leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which are also not disclosed or suggested in Wu, Mitchell, Sze, and Paterson.

Sze is cited by the Examiner to teach forming a dielectric by using a LPCVD process to provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput. Page 7 of the Final Rejection dated November 14, 2003. However, Sze also teaches that the LPCVD process has disadvantages, such as high temperature and low deposition rate. See, for example, page 211, Table 1 of Sze. Furthermore, Sze fails to teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process. Thus, Sze fails to remedy the basic deficiencies of Wu, Mitchell, and Yamagishi discussed above. In other words, Wu, Mitchell, and Yamagishi have failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which is also not disclosed or suggested in Sze.

Paterson is also cited by the Examiner to teach "a method of forming a semiconductor device, which includes depositing a high/temperature/quality oxide on the floating gate by LPCVD in order to provide high uniformity and a highly doped floating

gate (col. 3, lines 65-col. 4, lines 6 and col.4 line 67-col. 5, line 47)." Page 7 of the Final Rejection dated November 14, 2003. As discussed above, Paterson does not teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process. Furthermore, Paterson does not teach, disclose, or suggest utilizing an insulator formed by a LPCVD process and covering the sides of a floating gate such that the LPCVD-formed insulator prevents charge from leaking out of the sides of the floating gate.

Thus, Paterson fails to overcome the deficiencies of Wu, Mitchell, Yamagishi and Sze discussed above. In other words, Wu, Mitchell, Yamagishi, and Sze have failed to disclose or suggest depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking form the floating gate, and where the insulator layer is formed by a LPCVD process, which is also not disclosed or suggested in Paterson.

The Examiner has stated that it would have been obvious to use LPCVD oxide as taught by Sze or Paterson in the method of Wu or Mitchell in order to provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput. Page 7 of the Final Rejection dated November 14, 2003. The Appellant disagrees and submits that the Examiner has failed to provide any motivation that is disclosed or suggested in Wu or Mitchell to modify the method in Wu or Mitchell to specifically use

LPCVD oxide as taught by Sze or Paterson on the vertical side surfaces of the floating gate. Furthermore, any motivation to modify the method in Wu or Mitchell to use LPCVD oxide as taught by Sze or Paterson would have to be sufficiently strong in order to overcome the disadvantages of using a LPCVD process as also taught in Sze, such as high temperature and low deposition rate.

The Examiner has further stated that it would have been obvious to use a CMP method right after depositing the insulator as taught by Yamagishi in the method of Wu or Mitchell in order to simplify the overall processes and provide a planar surface. Page 9 of the Final Rejection dated November 14, 2003. Appellant disagrees and submits that the methods of Wu and Mitchell already provide a planar surface. Furthermore, Appellant submits that the Examiner has failed to show how using a CMP method right after depositing the insulator as taught by Yamagishi in the method of Wu or Mitchell would simplify the overall processes. Additionally, the Examiner has failed to provide any motivation that is disclosed or suggested in Wu or Mitchell to use a CMP method immediately after depositing the insulator.

Thus, considered together, the collective teachings of Wu, Mitchell, Yamagishi, Sze, and Paterson do not and cannot result in the present claimed invention. The purported combination of Wu, Mitchell, Yamagishi, Sze, and Paterson suggested by the Examiner is not based on anything that can be gleaned from the teachings of these references considered together. Rather, the teachings suggested by the Examiner are

based on a classic hindsight reconstruction given the benefit of Appellant's disclosure, which is impermissible.

For the foregoing reasons, Appellant respectfully submits that the present invention, as disclosed by independent claim 1, is not suggested, disclosed, or taught by Wu, Mitchell, Yamagishi, Sze, and Paterson, either singly or in any combination thereof. As such, the present invention, as defined by independent claim 1, is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson. Thus, claims 4-5 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The method of independent claim 7 teaches, among other things, depositing an insulator layer comprising a high temperature oxide directly on exposed portions of a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process, polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer. Independent claim 7 specifies limitations similar to those recited in independent claim 1. Thus, for similar reasons as discussed above, Appellant respectfully submits that the present invention, as defined by independent claim 7, is not suggested, disclosed, or taught by Wu, Mitchell, Yamagishi, Sze, and Paterson. As such, the present invention, as defined by independent

claim 7, is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson. Thus claims 9-11 and 14-15 depending from independent claim 7 are, *a fortiori*, also patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The method of independent claim 23 teaches, among other things, depositing an insulator layer comprising a high quality oxide directly on a tunnel oxide layer and a floating gate, where the insulator layer is formed on and in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and where the high quality oxide is formed by a LPCVD process, and polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer. Independent claim 23 specifies limitations similar to those recited in independent claim 1. Thus, for similar reasons as discussed above, Appellant respectfully submits that the present invention, as defined by independent claim 23, is not suggested, disclosed, or taught by Wu, Mitchell, Yamagishi, Sze, and Paterson. As such, the present invention, as defined by independent claim 23, is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson.

(3) The Rejection of Claims 14-15

Claims 14-15 stand rejected under 35 U.S.C. §103 as being unpatentable over Wu or Mitchell taken with Yamagishi and in view of Sze or Paterson as applied to claims 1, 4-5, 7, 9-11, and 23, and further in view of "Applicant's admitted prior art." As discussed above, the present invention, as defined by independent claim 7, is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson. Thus, claims 14-15 depending from independent claim 7 are, *a fortiori*, also patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 7, and 23 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 4-5, 7, 9-11, 14-15, and 23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 4-5, 7, 9-11, 14-15, and 23 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith in triplicate along with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 5/14/04

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APPENDIX OF CLAIMS ON APPEAL

Claim 1: A method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer comprising a high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, wherein the insulator layer is in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer is formed by a LPCVD process;

polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

Claim 4: The method of claim 1, wherein polishing the insulator layer includes using chemical mechanical polishing.

Claim 5: The method of claim 1, further comprising:

depositing a control gate layer on the ONO layer; and

etching the control gate layer and the ONO layer to form a stacked gate structure of the flash memory cell.

Claim 7: A method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide layer to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer comprising a high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate, wherein the insulator layer has a second thickness that is greater than the first thickness, wherein the insulator layer is in contact with vertical surfaces of the floating gate, and wherein the insulator layer is formed by a LPCVD process;

polishing the insulator layer immediately after the step of depositing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

Claim 9: The method of claim 7, wherein the first thickness of the floating gate layer is between approximately 500 Å and 2000 Å, and the second thickness of the insulator layer is between approximately 1000 Å and 5000 Å.

Claim 10: The method of claim 7, wherein polishing the insulator layer includes using chemical mechanical polishing.

Claim 11: The method of claim 7, further comprising:

depositing a control gate layer on the ONO layer; and

etching the control gate layer and the ONO layer to form a stacked gate structure of the flash memory cell.

Claim 14: The method of claim 7, wherein the floating gate layer comprises doped polysilicon.

Claim 15: The method of claim 7, wherein the floating gate layer comprises doped amorphous silicon.

Claim 23: A method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer comprising a high quality oxide directly on the tunnel oxide layer and the floating gate, wherein the insulator layer is deposited to a thickness greater than a thickness of the floating gate, wherein the insulator layer is formed on and in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the high quality oxide is formed by a LPCVD process;

polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing an ONO layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.